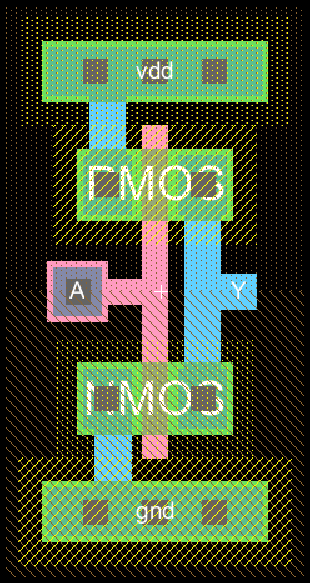
# VLSI Lab 5 – Full Adder

Matthew Murray – 873525242

## Not

A diagram of a circuit

AI-generated content may be incorrect.

### Logic Sim

A screen shot of a video game

AI-generated content may be incorrect.

Not\_out is high when va is low, and low when va is high.

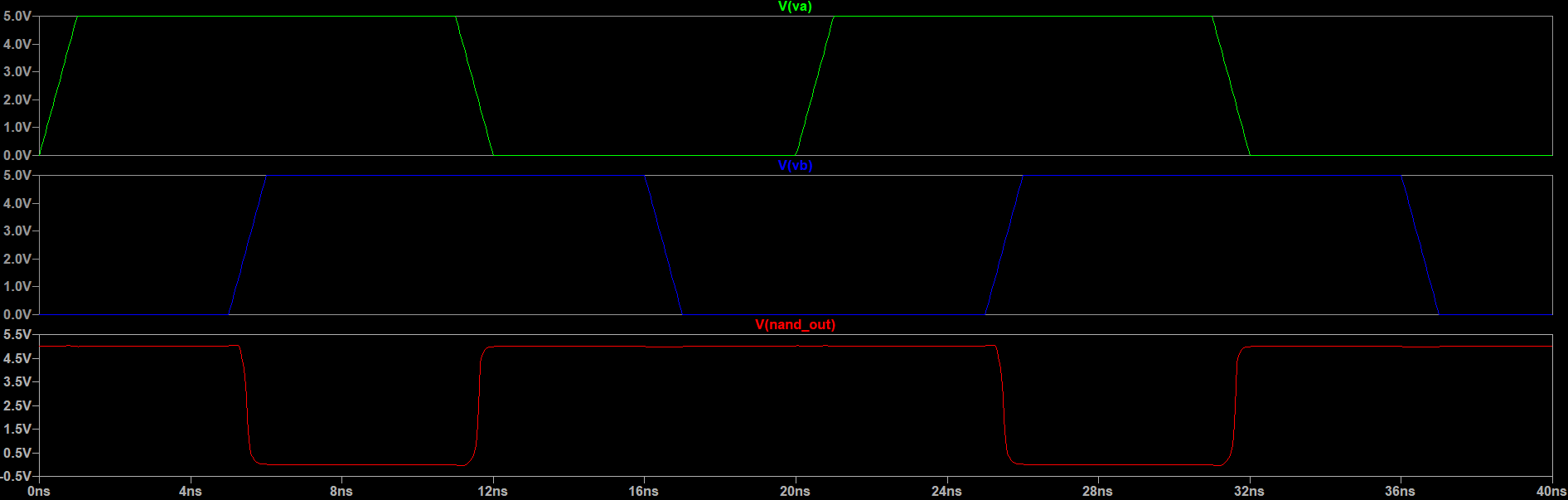
## NAND

A diagram of a circuit

AI-generated content may be incorrect.A screenshot of a cell phone

AI-generated content may be incorrect.

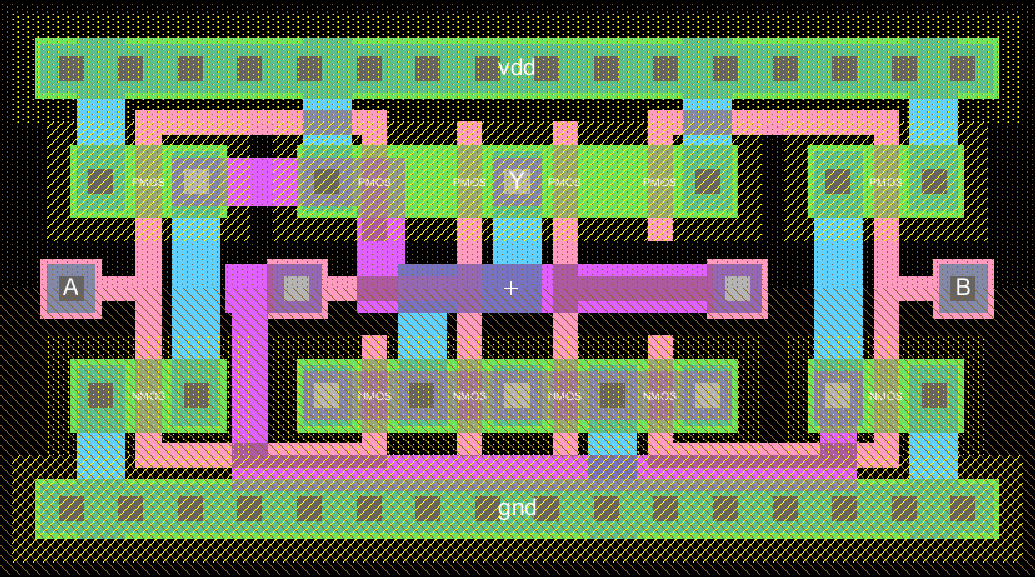
### Logic Sim



Nand\_out is low when both va and vb are high, and high otherwise.

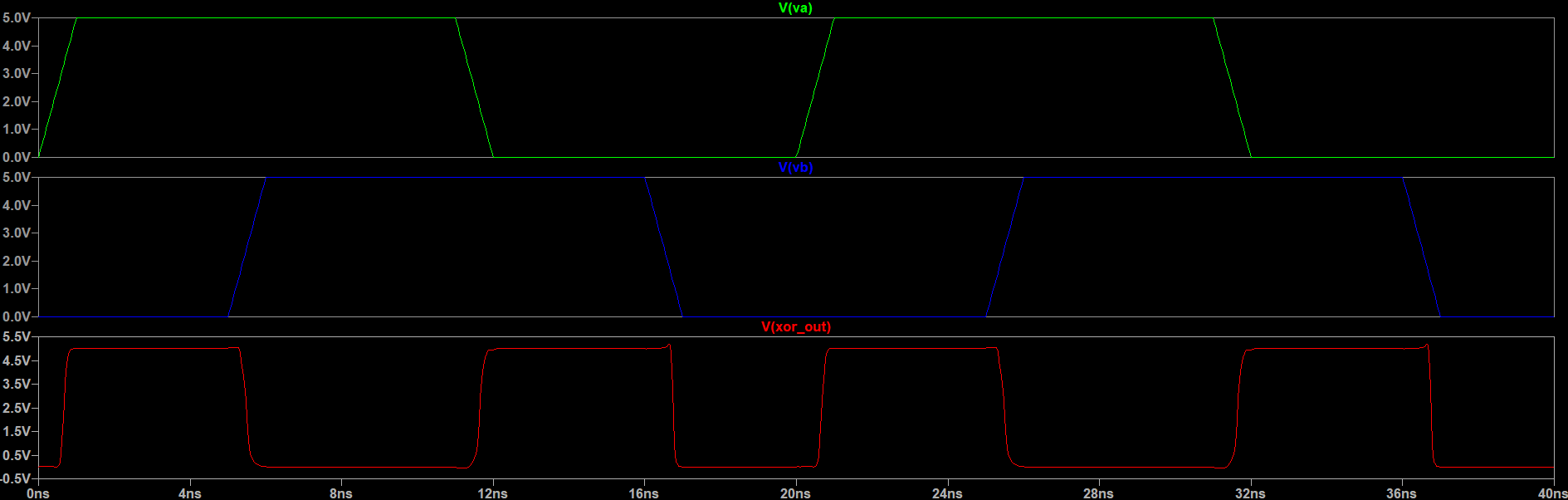
## XOR

A diagram of a circuit

AI-generated content may be incorrect.

Some nets were routed on metal 2 to keep the design as compact as possible. This way all the bulk connections will line up with the inverter and NAND bulk connections for the full adder.

### Logic Sim



Xor\_out is high when either va or vb are high, but not with both or neither or high.

### Output Glitches

A screen shot of a computer

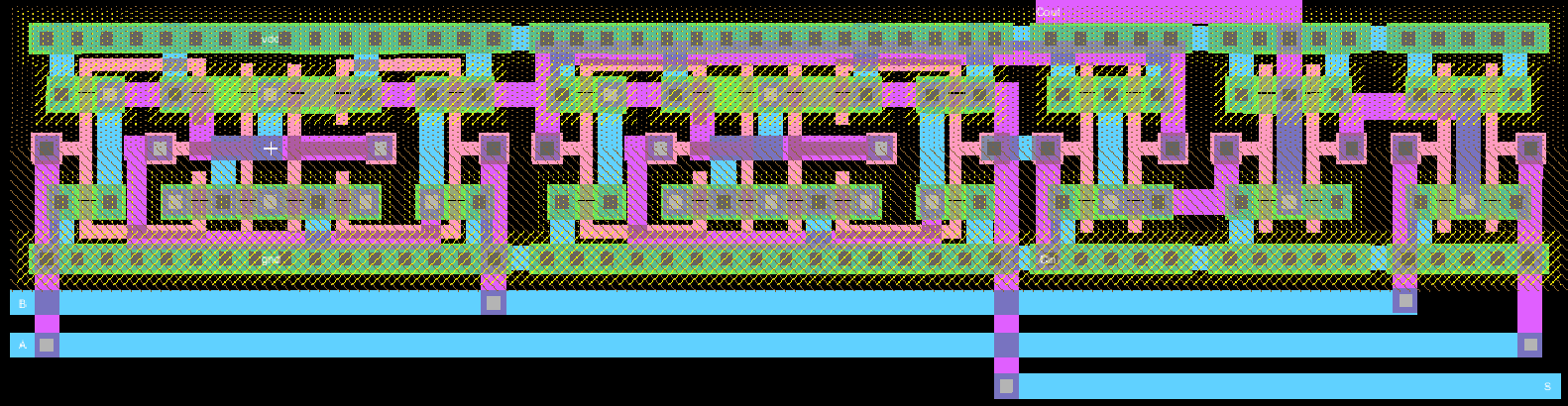
AI-generated content may be incorrect.

When both inputs change at the same time, the output can glitch in the transition zone like in the above simulation

## Full Adder

A screenshot of a computer

AI-generated content may be incorrect.



XORs

3 NANDs

The input and outputs are the bottom 3 metal 1 lines. If these could be placed on metal 3 they could be placed on top of the adder to make a fully tileable design.

### Logic Sim

A screen shot of a computer

AI-generated content may be incorrect.

S is high when either 1 or 3 of the inputs (a, b, cin) are high, otherwise its low. Cout is high when 2 or 3 of the inputs are high, otherwise its low.

### DRC & NCC

A white text with black text

AI-generated content may be incorrect.